NCP4331

Synchronous Buck Controller for High Efficiency Post Regulation

The NCP4331 houses a dual MOSFET driver intended to be used as a companion chip in ac-dc or dc-dc multi-output post regulated power supplies. Directly fed by the secondary ac signal, the device keeps power dissipation to the lowest while reducing external component count. Further, the implementation of N-channel MOSFETs gives NCP4331-based applications a significant advantage in terms of efficiency.

Features
- High Gate Drive Capability
- Bootstrap for N-MOSFET High-Side Drive
- Two Embedded Error Amplifiers Allowing Constant Current Constant Voltage (CCCV) Operation
- ±1.5% Regulation Voltage Reference Over 0°C to 85°C Temperature Range
- Programmable Soft-Start
- Thermal Shutdown for Overtemperature Protection
- PWM Operation Synchronized to the Converter Frequency
- Over-Lap Management for Soft Switching
- Internal Regulator to Ease the Circuit Feeding
- Undervoltage Detection
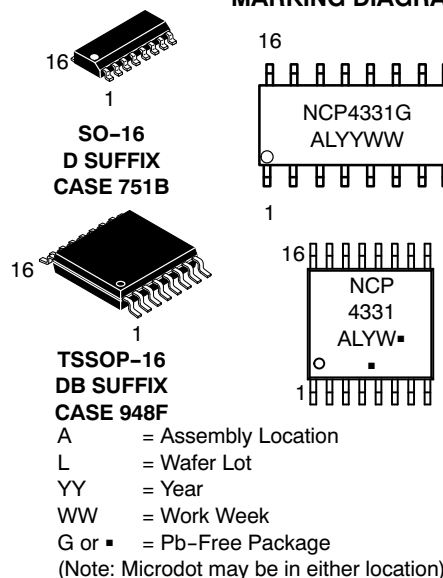- These are Pb-Free Devices

Typical Applications
- Off-line Switch Mode Power Supplies
- Power Dc-dc Converters
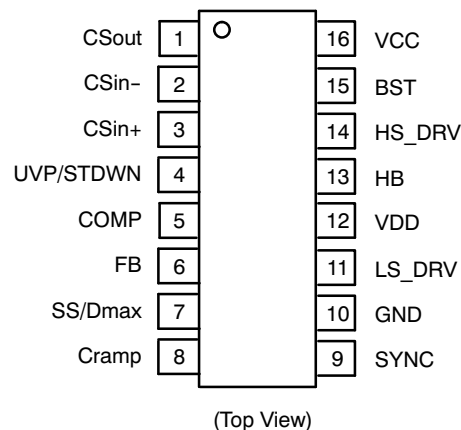- Efficient Alternative to Mag-Amp Post-Regulators

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAMS

SO-16
D SUFFIX
CASE 751B

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NCP4331G
ALYYWW
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TSSOP-16
DB SUFFIX
CASE 948F

```
NCP
4331
ALYW■
```

A = Assembly Location
L = Wafer Lot
YY = Year
WW = Work Week
G or ■ = Pb-Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS

CSout	1	16	VCC
CSin−	2	15	BST
CSin+	3	14	HS_DRV
UVP/STDWN	4	13	HB
COMP	5	12	VDD
FB	6	11	LS_DRV
SS/Dmax	7	10	GND
Cramp	8	9	SYNC

(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP4331DR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
NCP4331DBR2G	TSSOP-16 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
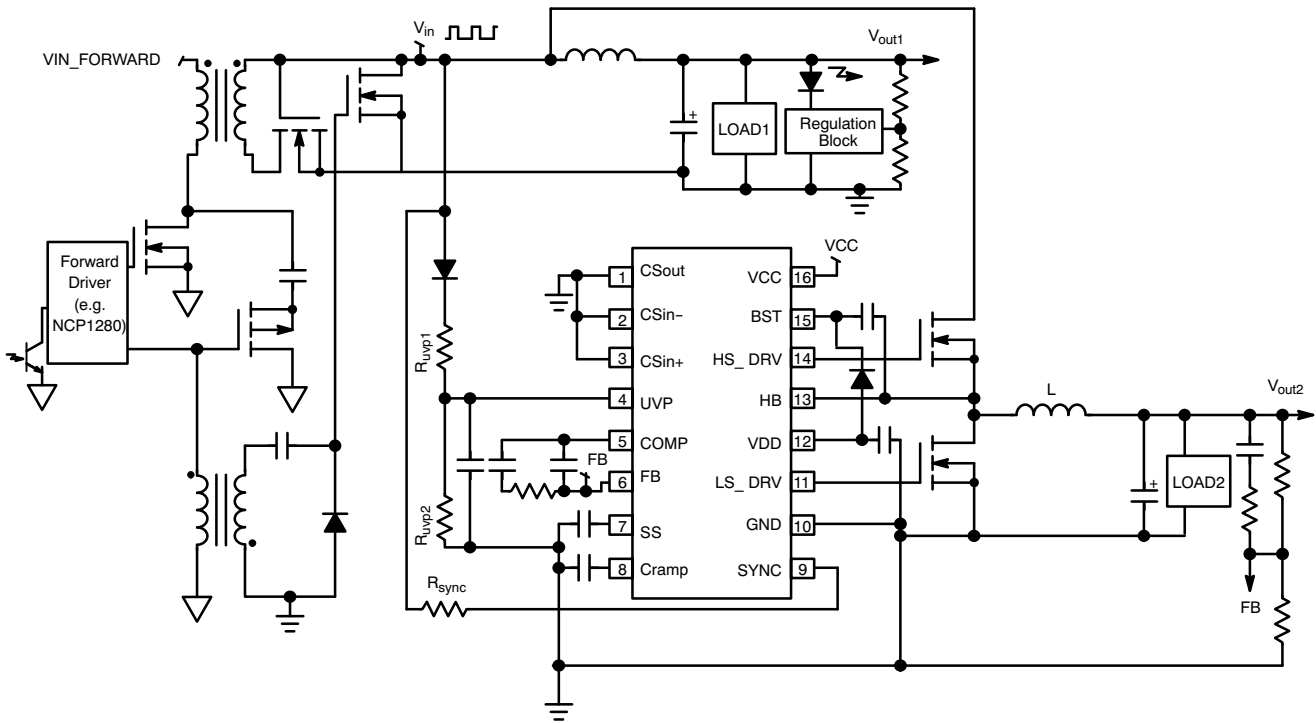
NCP4331

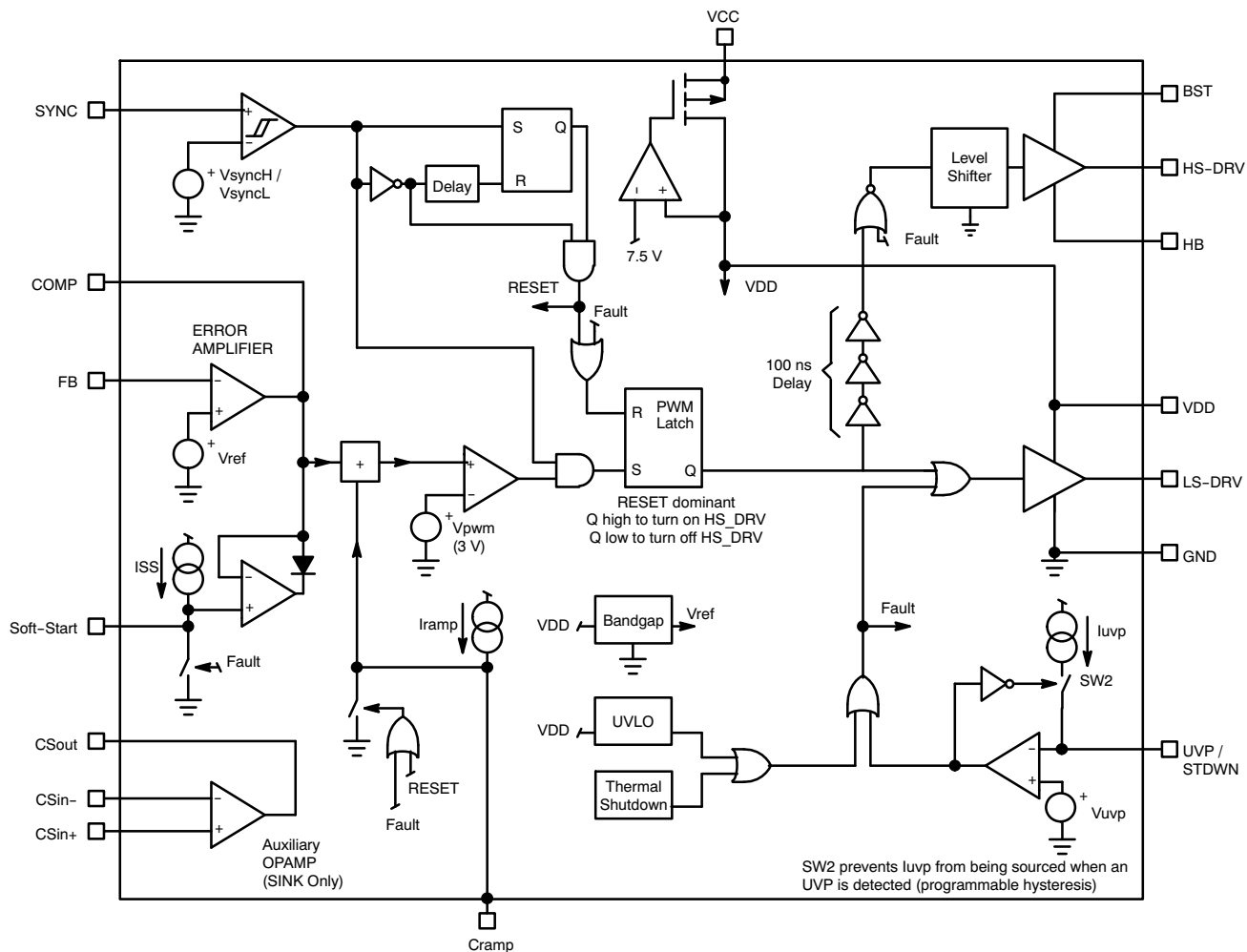**Figure 1. Typical Application Schematic**

NCP4331

Figure 2. Block Diagram

NCP4331

DETAILED PIN DESCRIPTIONS

Pin Number	Name	Function
1	CSout	Pin 1 is the output of the auxiliary error amplifier embedded in the NCP4331. This allows for the prevention of excessive coil or load current. Pin 1 can clamp the main error amplifier output. Controlling the coil current by this auxiliary error amplifier can provide a CCCV characteristic.
2	CSin–	Inverting input of the auxiliary error amplifier that is generally used to control the coil current.
3	CSin+	Noninverting input of the auxiliary error amplifier that is generally used to control the coil current.
4	UVP/ STDWN	This pin is designed to detect too low input voltage pulses and to turn off both the low–side and high–side drivers in such a faulty condition. Also, the soft–start pin is grounded so that the circuit smoothly recovers operation when the detected fault disappears. This UVP detection function features some programmable hysteresis to avoid erratic turns on and off of the device. Ground Pin 4 to shutdown the part.
5	COMP	This pin makes available the output of the internal error amplifier, for appropriate compensation of the regulation loop.
6	FB	Pin 6 is the feed–back pin that must receive a portion of the output voltage to regulate. It is connected to the inverting input of the internal error amplifier. The regulation reference is better $\pm 2\%$ over the –40°C to 125°C temperature range.
7	Soft–Start/ Dmax	Apply a capacitor to Pin 7 to slow down the start–up phase and reduce the stress during this sequence. Place a resistor between Pin 7 and ground to adjust the maximum duty–cycle of the high–side MOSFET. Combine the two functions by implementing these two components in parallel.
8	Cramp	This pin sources a constant current. Connect a capacitor to create a voltage ramp. This ramp is summed to the error amplifier output and compared to a constant voltage reference (V_{PWM}) to adjust the post–regulator duty–cycle.
9	SYNC	This pin is designed to receive a portion of the input voltage, to synchronize the post–regulator activity to its pulsed input voltage. Also, the high–side drive cannot be high state if the "SYNC" pin voltage is low.
10	GND	Ground pin of the circuit.
11	LS_DRV	"LS_DRV" is the driver output of the low–side MOSFET gate.
12	VDD	"VDD" is the circuit power source that is typically provided by the VCC Pin. A 0.1 μF to 1 μF ceramic capacitor should be connected between this pin and ground for decoupling.
13	HB	Connect the common node of the two MOSFETs to this pin.
14	HS_DRV	"HS_DRV" is the driver output of the high–side MOSFET gate.
15	BST	"BST" is the bootstrap pin. A 0.1 μF to 1 μF ceramic capacitor should be connected between this pin and the "HB" node. The "BST" voltage feeds the high–side driver ("HS_DRV").
16	VCC	A DC voltage (up to 30 V) must be applied to this pin. This voltage is internally post–regulated down to 7.5 V to provide the V_{DD} voltage that powers the circuit.

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
BST, HB	Bootstrap and "Half–Bridge" Node Inputs (Referenced to GND)	−2, +40	V
BST_{HB}	Bootstrap Pin Voltage Referenced to the HB Node	−0.3, +10	V
V_{CC}	Internal Regulator Input	−0.3, +30	V
V_{in}	Pins 1, 2, 3, 4, 5, 6, 7, 8 and 9	−0.3, +5	V
V_{DD}	Supply Voltage	−0.3, +10	V
$R_{\theta JA}$	Thermal Resistance (TSSOP–16 and SOIC–16)	145	°C/W
	ESD Capability, Human Body Model (HBM)	2	kV
	ESD Capability, Machine Model (MM) (Note 2)	200	V
T_A	Operating Temperature Range (Note 1)	−40, +125	°C
T_{Jmax}	Maximum Junction Temperature	150	°C
T_{Smax}	Storage Temperature Range	−65 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. The maximum junction temperature should not be exceeded.
2. The Machine Model ESD capability is 150 V for Pin 9.

ELECTRICAL CHARACTERISTICS (V_{CC} = 20 V, V_{BST} = 7 V, HB Grounded, T_J = 0°C to +125°C, unless otherwise specified)

Symbol	Rating	Min	Typ	Max	Unit
HIGH–SIDE OUTPUT STAGE					
R_{HS_source}	Source Resistance @ I_{source} = 100 mA	–	3	6	Ω
R_{HS_sink}	Sink Resistance @ I_{sink} = 100 mA	–	2	4	Ω
t_{r-HS} t_{f-HS}	Rise and Fall Times: High–Side Output Voltage Rise Time (C_L = 1 nF) (Note 3) High–Side Output Voltage Fall Time (C_L = 1 nF) (Note 3)	– –	13 8	20 15	ns
T_{LS-HS}	Delay from Low–Side Gate Drive Low (High) to High–Side Drive High (Low) (Note 6)	35	55	75	ns
LOW–SIDE OUTPUT STAGE					
R_{LS_source}	Source Resistance @ I_{source} = 100 mA	–	3	6	Ω
R_{LS_sink}	Sink Resistance @ I_{sink} = 100 mA	–	2	4	Ω
t_{r-LS} t_{f-LS}	Rise and Fall Times: High–Side Output Voltage Rise Time (C_L = 1 nF) (Note 3) High–Side Output Voltage Fall Time (C_L = 1 nF) (Note 3)	– –	13 8	20 15	ns
CURRENT CONTROL ERROR AMPLIFIER (Auxiliary Error Amplifier)					
IB_{pin3}	Noninverting Input Bias Current @ V_{pin3} = V_{pin2} = V_{ref}	−500	−100	0	nA
IB_{pin2}	Inverting Input Bias Current @ V_{pin3} = V_{pin2} = V_{ref}	−500	−100	0	nA
V_{io}	Input Offset Voltage (Note 5)	−5	1	5	mV
BW	Gain Bandwidth	–	4	–	MHz
G_{EA}	Open Loop Voltage Gain	–	70	–	dB
V_{LL}	Pin 1 Voltage if V_{pin2} = 1 V and V_{pin3} = 0 V, 100 μA Being Sourced Into Pin 1	0	–	0.5	V

3. The risetime is the time needed by the drive to go from 10% to 90% of the supply voltage. The fall time is the time required by the drive to drop from 90% to 10% of its supply voltage. These times are not tested in production but only guaranteed by design.
4. Guaranteed by design. Tested through the R_{RESET} parameter.
5. Guaranteed by characterization and design.
6. This delay is specified with the HB pin being grounded. In typical application where the HB node is pulsing, the delay is 70 ns typically

ELECTRICAL CHARACTERISTICS (V_{CC} = 20 V, V_{BST} = 7 V, HB Grounded, T_J = 0°C to +125°C, unless otherwise specified)

Symbol	Rating	Min	Typ	Max	Unit
ERROR AMPLIFIER					
V_{ref}	Referenced Voltage Regulation @ Pin 7 Being Open 0°C < T_J < 85°C −40°C < T_J < 125°C (Guaranteed by Test from 0°C < T_J < 125°C and Extended to −40°C by Design)	0.738 0.735	0.750 0.750	0.762 0.765	V
IB_{FB}	Feedback Input Bias Current @ V_{pin6} = V_{ref}	−500	−250	0	nA
BW	Gain Bandwidth	–	4	–	MHz
G_{EA}	Open Loop Voltage Gain	–	70	–	dB
EA_{out} −EA_{max} −EA_{min}	Pin 5 (Compensation) Voltage V_{pin6} = 0 V V_{pin6} = 1 V	3.50 –	3.70 0.05	– 0.50	V
$I_{source-EA}$	Output Source Current @ V_{pin6} = 0 V	40	65	90	μA
SOFT−START AND MAXIMUM DUTY−CYCLE LIMITATION (D_{max})					
I_{SS}	Source Current @ V_{SS} = 0 V to 3.5 V	40	50	63	μA
V_{SS}	Clamp Voltage	3.5	3.7	–	V
EA_{MIN}	Error Amplifier Output @ V_{pin5} = 0.5 V	–	0.05	0.5	V
EA_{SS}	Error Amplifier Output @ V_{pin6} = 0 V and V_{pin7} = 2 V	1.9	2.0	2.1	V
RAMP CONTROL					
I_{ramp}	C_{ramp} Current Source @ V_{ramp} = 0 V to 3.5 V	40	50	63	μA
V_{rampH}	C_{ramp} Ramp Clamp	3.5	3.7	–	V
V_{rampL}	Low Voltage of the Ramp Saw−Tooth	–	–	100	mV
V_{rampON}	Ramp Voltage Enabling the High−Side Driver: @V_{pin5} = 0.5 V @ V_{pin5} = 3.5 V (Min Highest EA Value) @ V_{pin5} = 2 V	2.30 – 0.80	2.50 – 1.00	2.65 0 1.20	V
Q_{RESET}	Current Charge Extracted During the RESET Pulse (Note 4)	5	–	–	nC
T_{RESET}	Delay from SYNC Pin low to Reset Completion (a Falling Pulse Being Applied to Pin 16)	–	200	350	ns
R_{RESET}	Sink Resistance of Pin 8 during the Reset Time @ I_{pin8} = 10 mA (This is the Resistance of the Switch that Discharges the C_{ramp} Capacitor during the Reset Pulse − Capability of 5 nC Min)	–	15	25	Ω
SYNCHRONIZATION BLOCK					
$V_{SYNC}H$	Synchronization Comparator Threshold (V_{pin9} Rising)	2.4	2.5	2.6	V
H_{SYNC}	Synchronization Comparator Hysteresis	1.2	1.5	1.8	V
$V_{CL-SYNC}$	Negative Clamp Voltage of the Synchronization Pin @ I_{pin16} = 2 mA	−0.3	–	0	V
$T_{SYNC \geq HS}$	Delay From SYNC Pin High to HS_DRV High (A Rising PUlse Being Applied to Pin 16)	–	100	250	ns
UNDERVOLTAGE DETECTION (UVP)/SHUTDOWN					
$V_{UVP}L$	Comparator Threshold (V_{pin4} Being Falling)	1.92	2.00	2.08	V
$V_{UVP}H$	Comparator Threshold (V_{pin4} Being Rising) (Note 5)	–	–	2.20	V
H_{UVP}	Hysteresis of the UVP Comparator	–	40	–	mV
I_{UVP}	UVP Current Source	15	25	30	μA
IB_{UVP}	Bias Current	–	–	0.1	μA

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6. This delay is specified with the HB pin being grounded. In typical application where the HB node is pulsing, the delay is 70 ns typically

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ELECTRICAL CHARACTERISTICS (V_{CC} = 20 V, V_{BST} = 7 V, HB Grounded, T_J = 0°C to +125°C, unless otherwise specified)

Symbol	Rating	Min	Typ	Max	Unit
TEMPERATURE PROTECTION					
T_{LIMIT}	Thermal Shutdown Threshold (Note 5)	150	160	170	°C
H_{TEMP}	Thermal Shutdown Hysteresis	–	50	–	°C
V_{CC} BIASING (Internal Voltage Regulator)					
$I_{VCC-max}$	Regulator Current Limitation	–	60	–	mA
V_{DD}	V_{DD} Voltage @ V_{CC} = 20 V and I_{VDD} = 20 mA	7.0	7.5	8.0	V
V_{DROP}	Voltage Drop Between the V_{CC} and V_{DD} Pin @ I_{VCC} = 20 mA	–	0.17	1.0	V
I_{CC}	Operating Consumption: No Switching (Fault Mode) Switching (100 kHz)	– –	1.5 2.0	1.9 4.0	mA
V_{DD} MANAGEMENT					
UVD_H	Undervoltage Lockout Threshold (V_{DD} rising)	5.3	6.0	6.7	V
UVD_L	Undervoltage Lockout Threshold (V_{DD} falling)	5.0	5.6	6.2	V
H_{UVD}	Undervoltage Lockout Hysteresis	300	400	–	mV

3. The risetime is the time needed by the drive to go from 10% to 90% of the supply voltage. The fall time is the time required by the drive to drop from 90% to 10% of its supply voltage. These times are not tested in production but only guaranteed by design.
4. Guaranteed by design. Tested through the R_{RESET} parameter.
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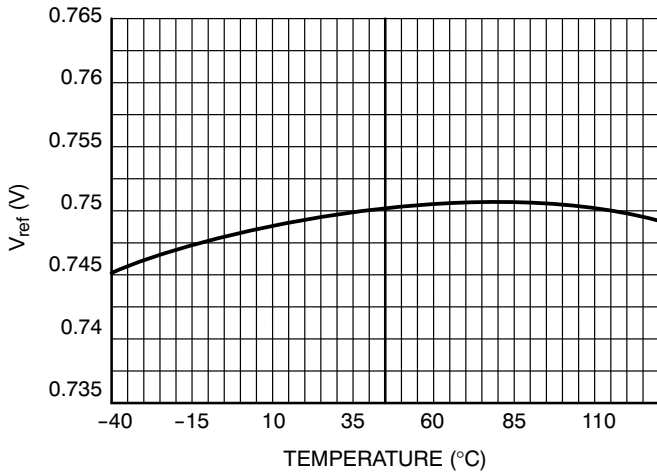
Figure 3. Regulation Voltage Reference (V$_{ref}$) versus Temperature
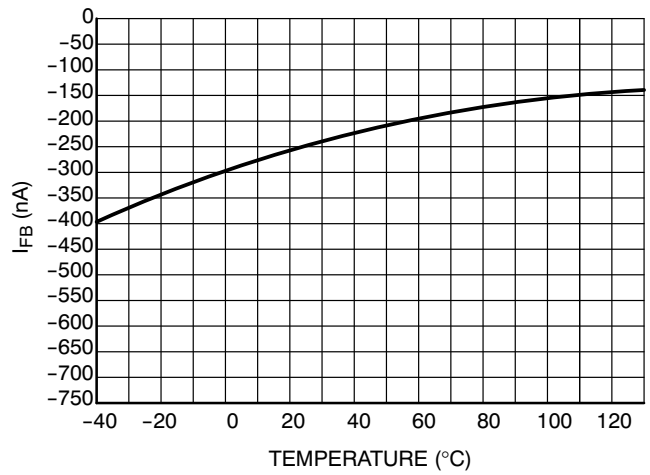
Figure 4. FB Pin Bias Current versus Temperature
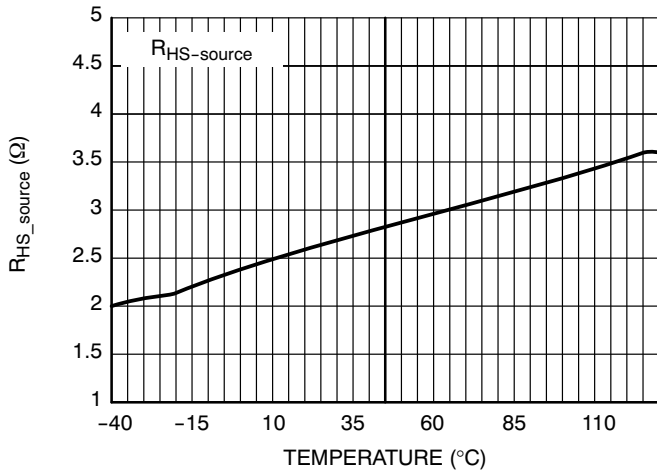
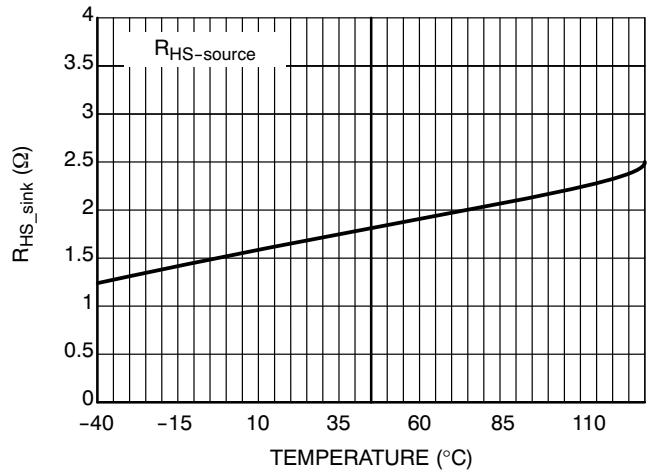**Figure 5. Source Resistance of the High–Side Output @ I$_{source}$ = 100 mA versus Temperature**

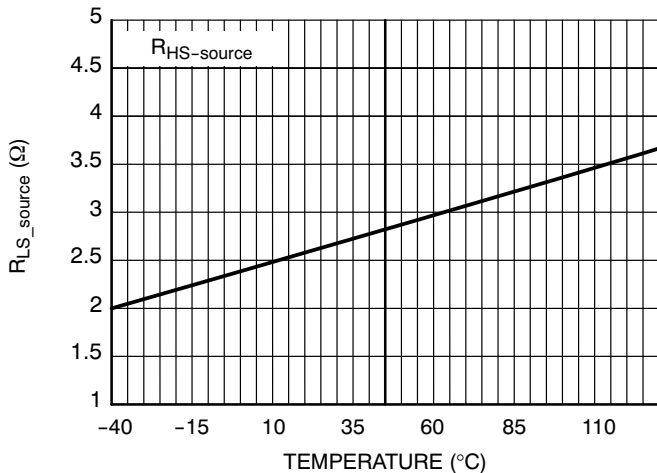**Figure 6. Sink Resistance of the High–Side Output @ I$_{sink}$ = 100 mA versus Temperature**

Figure 7. Source Resistance of the Low–Side Output @ I$_{source}$ = 100 mA versus Temperature
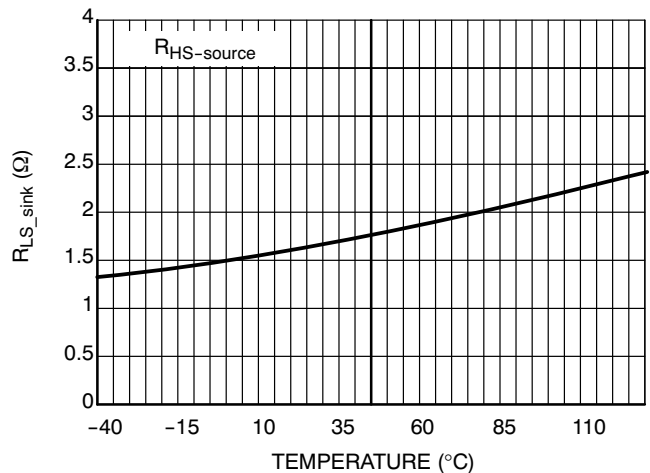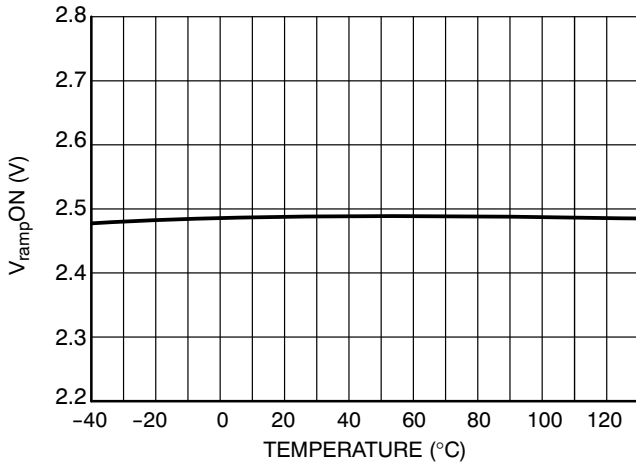

Figure 8. Sink Resistance of the Low–Side Output @ I$_{sink}$ = 100 mA versus Temperature

Figure 9. V$_{ramp}$ON versus Temperature @ V$_{pin5}$ = 0.5 V
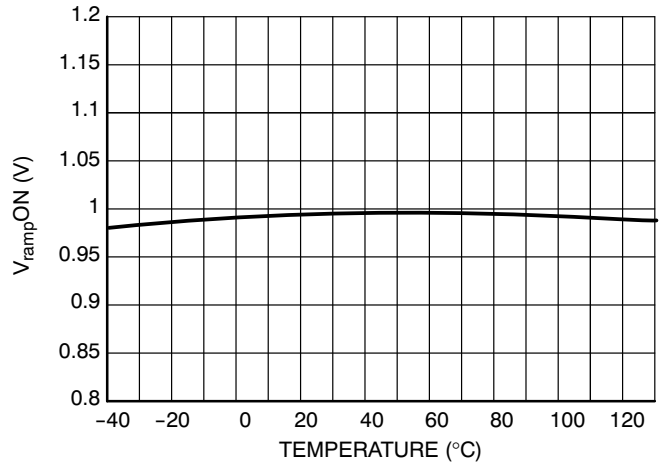
Figure 10. V$_{ramp}$ON versus Temperature @ V$_{pin5}$ = 2.0 V
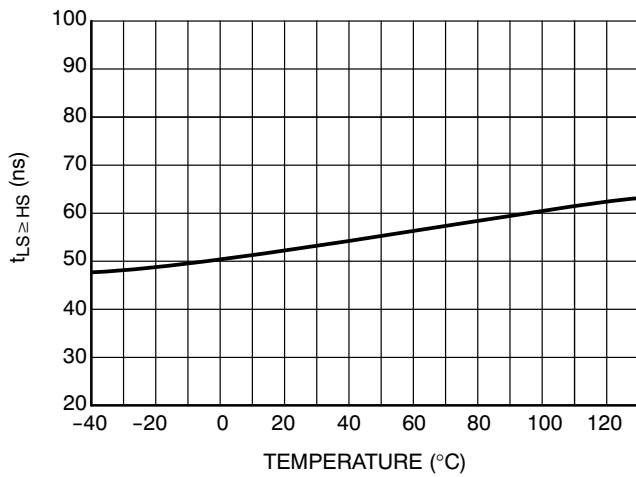
Figure 11. Low–Side to High–Side Delay versus Temperature, High–Side Falling
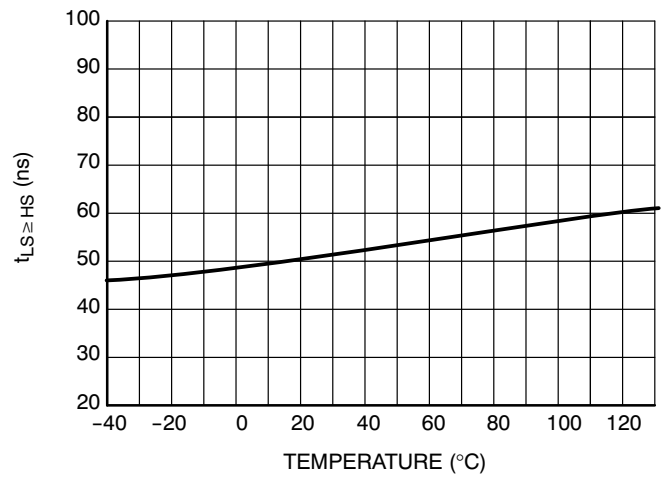
Figure 12. Low–Side to High–Side Delay versus Temperature, High–Side Rising
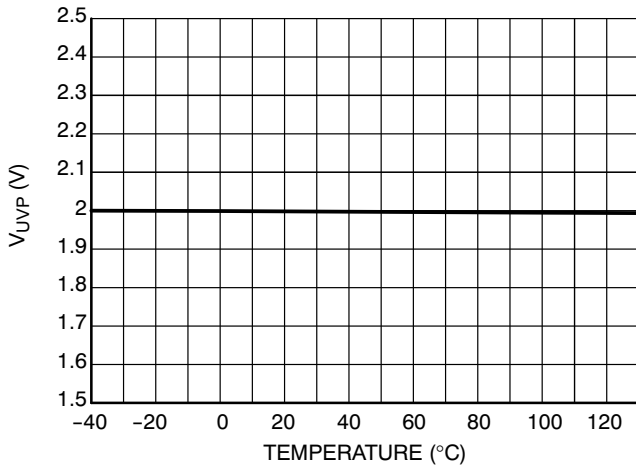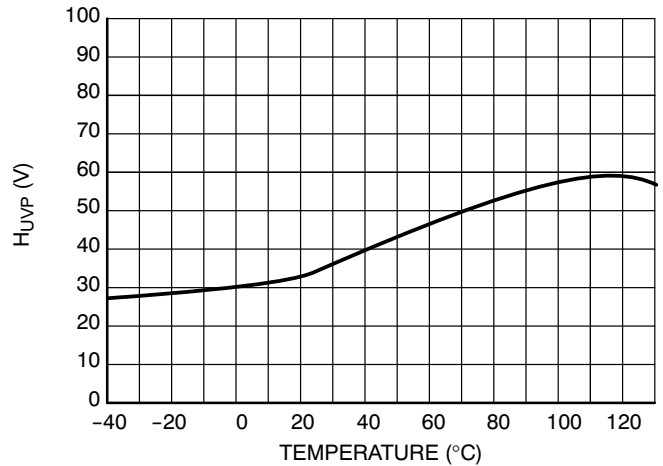

Figure 13. UVP Threshold versus Temperature

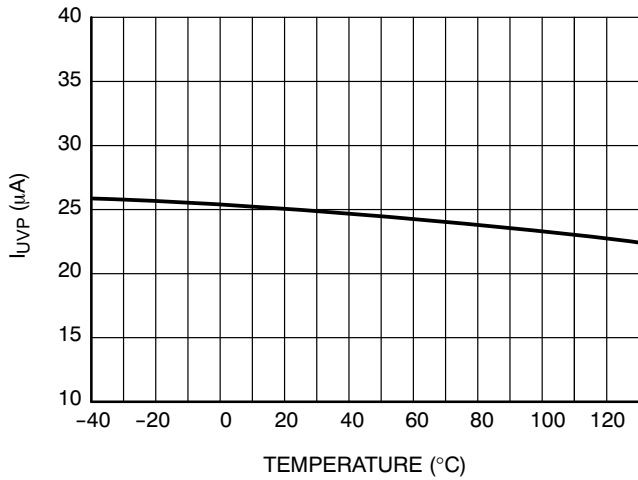**Figure 14. Hysteresis of the UVP Comparator versus Temperature**

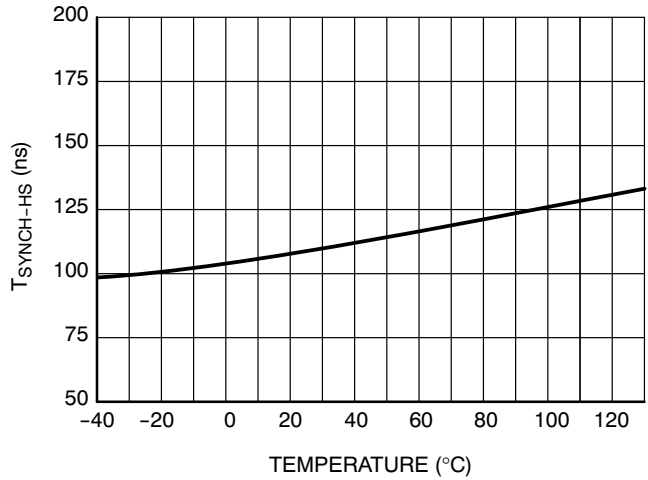**Figure 15. UVP Current Source versus Temperature**

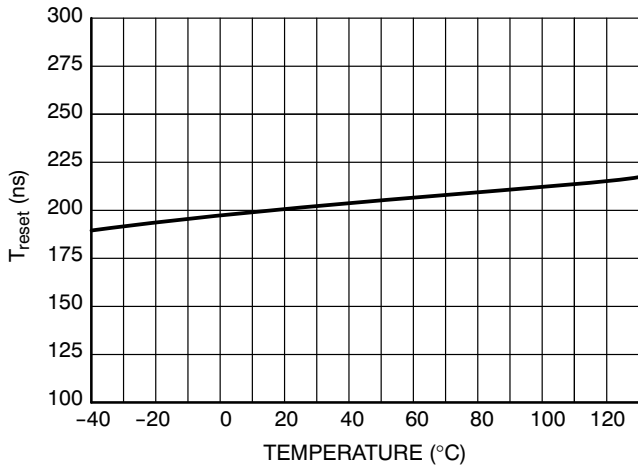**Figure 16. Delay Synchronization Pulse to HS High versus Temperature**
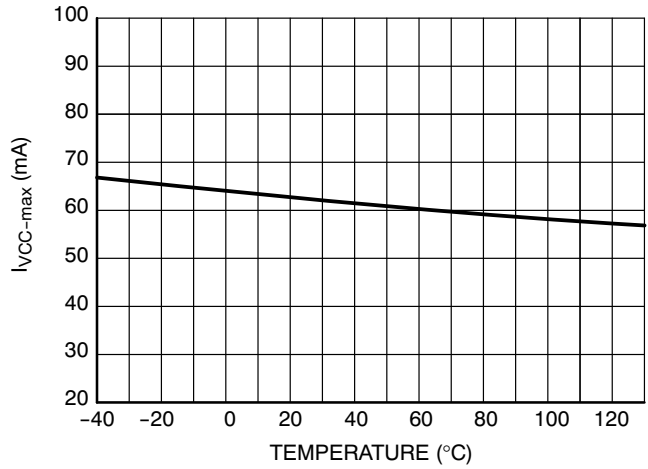
Figure 17. Reset Time versus Temperature

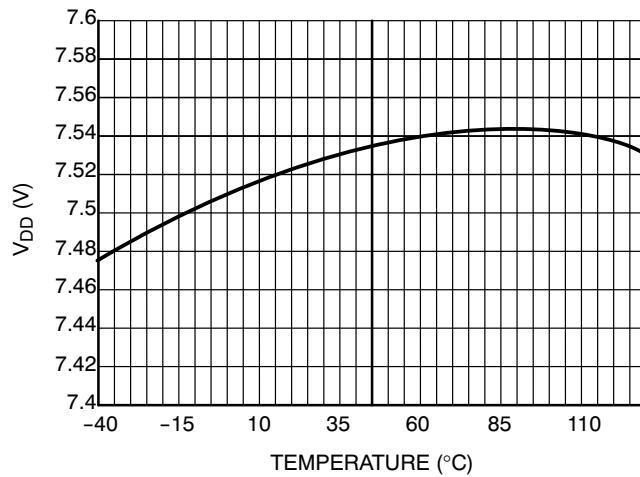**Figure 18. Current Limitation of the V$_{CC}$ Internal Regulator versus Temperature**

Figure 19. V$_{DD}$ Voltage versus Temperature @ V$_{cc}$ = 20 V and I$_{VDD}$ = 20 mA

DETAILED OPERATING DESCRIPTION

Introduction

The NCP4331 is ideal in multi-outputs applications where efficiency, ease of implementation and compactness are key requirements. Since it is often impossible to tightly regulate all the outputs and since a further regulation of the outputs is not an efficient option, it is preferable to do as follows:

- Traditionally regulate the highest output voltage.

- Post-regulate the other ones, by directly drawing the energy from the transformer secondary ac voltage. The NCP4331 is a controller developed to drive such buck converters that have the ability to operate from pulsed voltage.

Typically, NCP4331 driven post-regulators are associated to forward converters as portrayed by Figure 20. For the sake of the simplicity, the forward of Figure 20 consists of a simple demagnetization winding and output diodes, but more sophisticated options including active clamp and synchronous rectification, would lead to a better global efficiency of the solution.

Also, one can associate the NCP4331 to other architectures (like two switches' forward or half-bridge converters). Any converter able to provide the NCP4331 post-regulator with a square wave source could use this concept, as long as the NCP4331 maximum ratings are not exceeded (in particular, the "BST" and "HB" maximum voltage).

Finally, the NCP4331 has the following main benefits:

- **Efficiency:** The NCP4331 concept avoids the implementation of downstream converters to re-process the main converter output voltage when two or more outputs are to be tightly regulated. Instead, like Mag-amp systems, NCP4331 driven post-regulators directly draw the energy from the secondary side of the main converter transformer, for a more efficient power processing. In addition, the circuit manages the sequencing in a smart manner so that three over the four transitions are soft. The high gate drive capability of the NCP4331 and the utilization of N-MOSFETs for both the high and low sides reduce the conduction losses to a minimum (synchronous rectification).

- **Ease of implementation and compactness:** The NCP4331 is housed in a small SO16 package and it incorporates all the functions necessary for a reliable post-regulation (synchronization block, accurate regulation block, soft-start, current control). Hence, NCP4331 driven post-regulation requires few external components. Also the high switching frequency levels it can handle (up to 400 kHz) allows the utilization of small output coil and capacitor. An internal regulator highly eases the circuit feeding.

- **Robustness:** The NCP4331 embeds powerful features to protect the application from possible over-stresses and make the post-regulator very rugged. In particular, it incorporates a second operational amplifier to lower the duty-cycle and ultimately clamp the coil current when it tends to become excessive (CCCV characteristic). Also, the soft-start and the undervoltage protections improve reliability. In addition, they help control the start and end of the post-regulator operation. Ultimately, the integration within the whole system is eased.

Post-Regulation Operation

Figure 20 illustrates the concept where two outputs are to be regulated ("V_{out1}" and "V_{out2}"). The highest output (V_{out1}) is traditionally regulated thanks to a regulation arrangement that modulates the forward converter duty cycle. The other output (V_{out2}) is regulated by a dual MOSFET arrangement driven by the NCP4331. The high-side MOSFET turns on during one part of the forward converter on-time, while the low-side power switch is ON for the rest of the period (free wheeling).
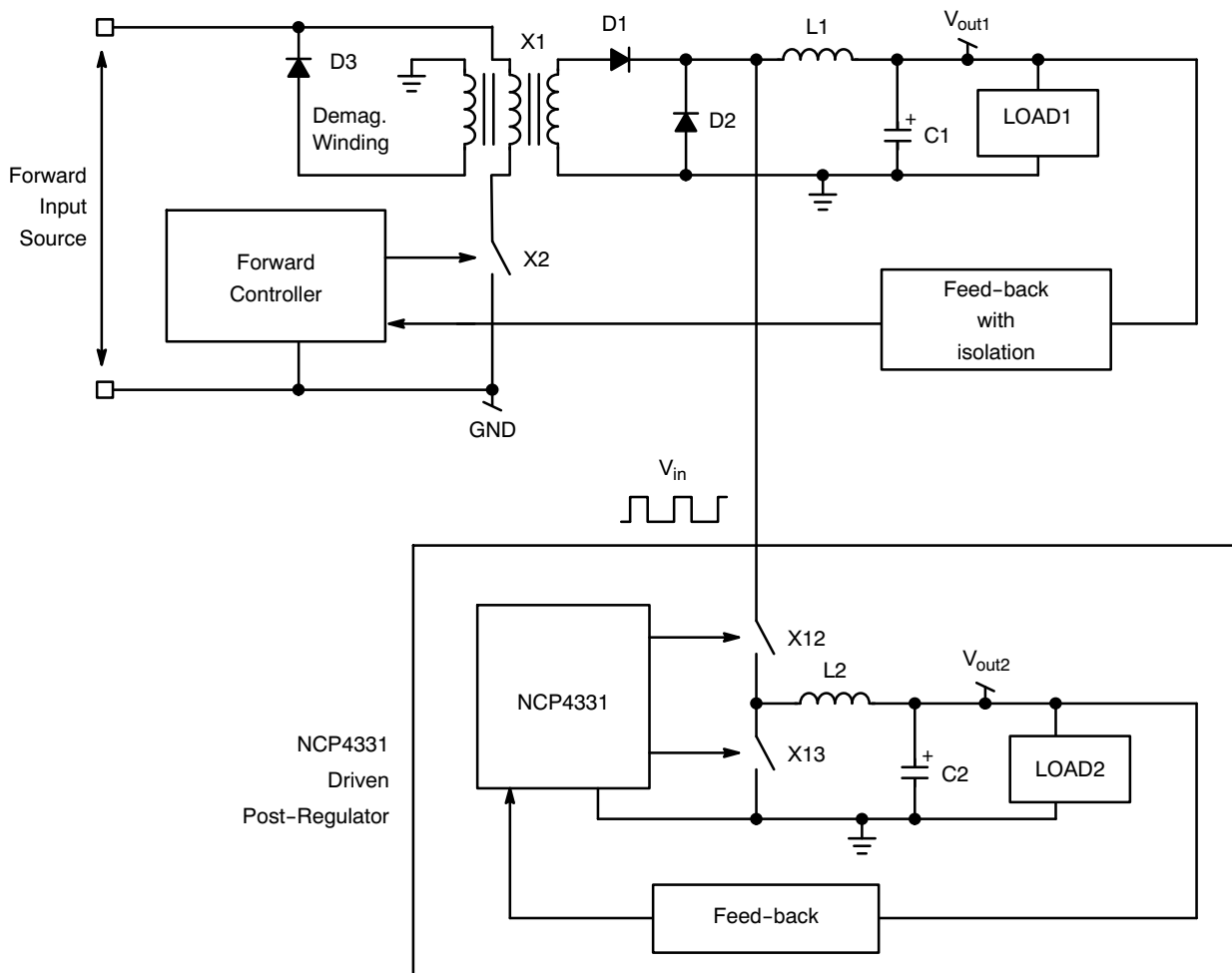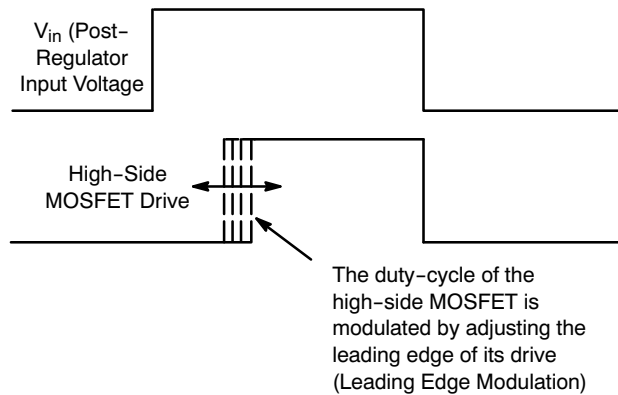
Figure 20. NCP4331 Post−Regulator Associated to a Forward Converter

In the case of a forward operating in continuous conduction mode (CCM) operation, the cycle is simply given by the following equation (the converter losses being neglected):

$$d_F = \frac{V_{out1}}{\left(\frac{N_S}{N_P}\right) \cdot (V_{in})_{forward}}$$

(eq. 1)

Where:

d_F is the forward duty cycle,

N_S/N_P is the transformer turn ratio (N_P: primary number of turns, N_S: secondary number of turns),

$(V_{in})_{forward}$ is the forward converter input voltage,

V_{out1} is the main output voltage of the forward converter.

The duty-cycle of the high-side MOSFET is modulated by adjusting the leading edge of its drive (Leading Edge Modulation)

Figure 21. Leading Edge Modulation

As portrayed in Figure 21, the post-regulator controls the energy to be drawn from the power source V_{in} by adjusting the time during which the high-side MOSFET is on. This conduction time is modulated by adjusting the leading edge of the high side drive while the trailing edge stays synchronized to the input voltage V_{in}.

As in a traditional buck, the post-regulated output voltage is given by the following equation:

$$V_{out} = d_n \cdot \frac{N_S}{N_P} \cdot \left(V_{in}\right)_{forward} \qquad \text{(eq. 2)}$$

Sequencing and Regulation Block

The following timing diagram portrays the sequencing.

Where: d_n is the duty cycle of the post-regulator n.
$d_n < d_F$ since $(N_S/N_P \bullet (V_{in})_{forward})$ is available only during the forward converter on-time and that anyway, the high-side MOSFET cannot be turn on as long as V_{in} is low (i.e., during the forward off-time).

Post-regulated output voltages are then necessarily lower than the main regulated one. However, the NCP4331 scheme allows d_n to nearly equal d_f so that if necessary, a post-regulated output voltage ($Vout_n$) can be very closed the main one (V_{out1}).
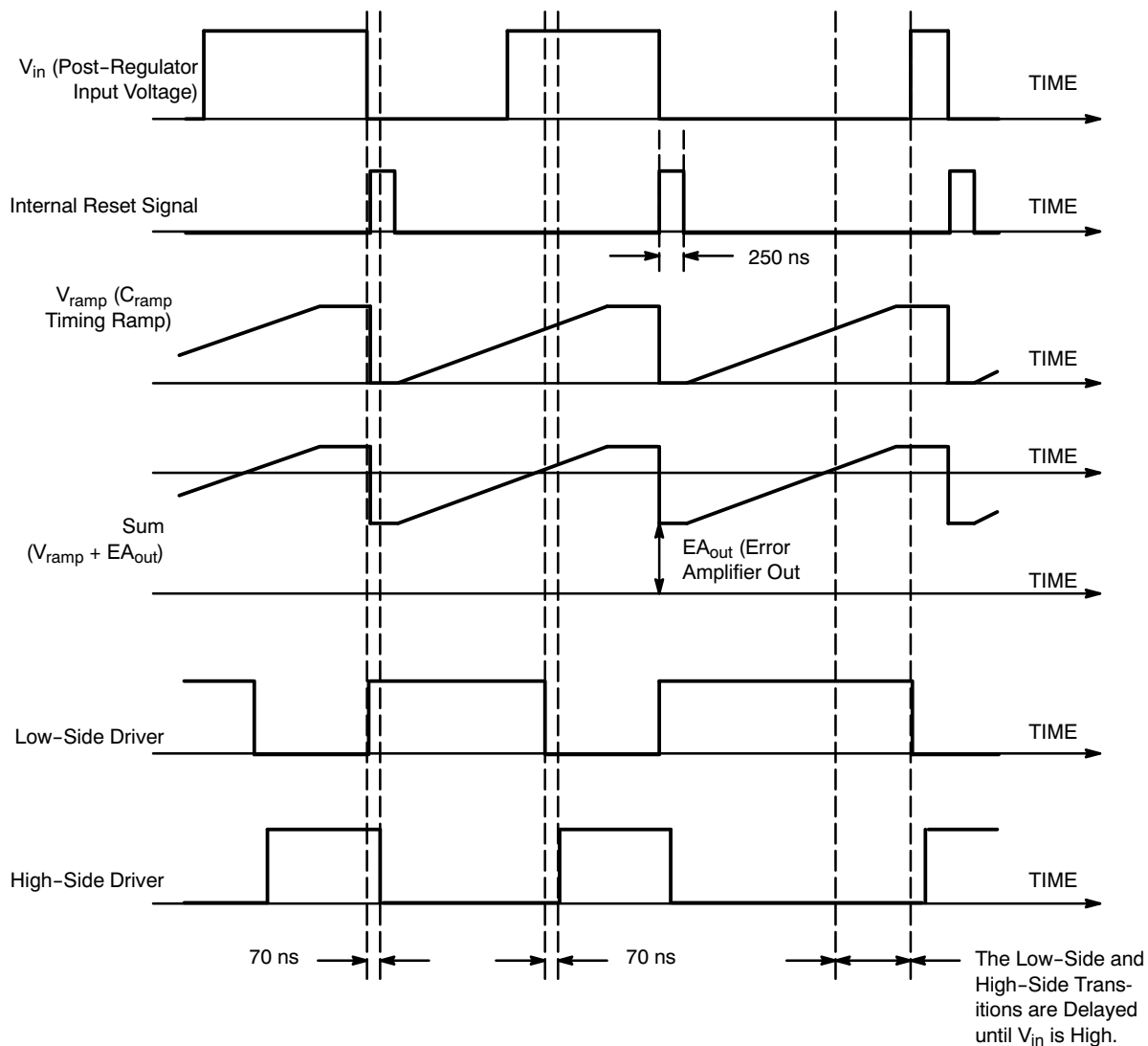

Figure 22. Timing Diagram

Sequencing and Overlapping

Figure 22 portrays the sequencing of a NCP4331 driven post-regulator.

The high-side driver turns on (off) after some delay just after the low-side has switched off (on). More precisely, the high-side MOSFET:

- Turns on 70 ns after the low–side MOSFET opening,
- Turns off 70 ns after the low–side MOSFET closing.

Hence, there are 70 ns when both the high–side and low–side MOSFETs are on. Such a behavior is possible because this event occurs just after the input voltage has dropped to zero (the post–regulator is not the seat of cross–conduction and instead, as it will be seen in next sections, this sequencing optimizes the switching performance), i.e., at the beginning of the forward free wheeling phase. Hence, no energy can then be drawn from the converter transformer during this delay and these 70 ns should not be considered as a part of the high–side MOSFET conduction time.

Similarly, there are 70 ns during which both MOSFETs are off, just before the low side conduction phase. During this short time, the body diode of the low side MOSFET derives the coil current. Hence, its drain–source voltage is already low when the low–side MOSFET turns on. The resulting Zero Voltage Switching optimizes the efficiency.

In light load, the body diode of the high–side MOSFET may conduct the coil current if it is negative (flowing back from the load to the input).

Error Amplifier

The NCP4331 embeds an error amplifier. The internal 0.75 V reference is better than ±1.5% accurate over the 0°C to 85°C temperature range (±2% over the 0°C to 85°C range). The circuit provides access to its inverting input and to its output. Typically, the output voltage of the post–regulator is scaled down by a resistive divider to be monitored by the inverting input ("FB" pin – Pin 6). The bias current is minimized (less than 500 nA) to allow the use of a relatively high impedance feed–back network. The output of the error amplifier is pinned out for external loop compensation (Pin 5). Please note that a NCP4331 driven post–regulator can be viewed as a voltage mode buck converter and hence, that a type 3 compensation network is recommended (see application schematic of page 1).

Ramp Generation and PWM Section

An internal current source (I_{RAMP} = 50 μA) charges the C_{RAMP} timing capacitor to form a ramp that is reset by the synchronization pin when the input voltage falls down. The circuit adds the resulting, synchronized saw–tooth (V_{ramp}) to the error amplifier output (EA_{OUT}). The PWM comparator monitors the obtained sum and sets the PWM latch when this voltage (V_{ramp}+ EA_{OUT}) exceeds the internal PWM reference ("V_{PWM}"). As a consequence, the low–side MOSFET turns off. 70 ns later, the high–side MOSFET switches on and remains closed until the next RESET sequence, i.e., when the input voltage drops to zero. Hence, the raising edge of the high–side MOSFET is modulated by the moment when the sum crosses the PWM reference. In other words, the NCP4331 operates in the so called Leading Edge Modulation. In fact, the PWM latch cannot be set before the input voltage is in high state. This is to avoid that the high–side MOSFET is on while there is

no input voltage. Also, this feature prevents the high–side MOSFET from keeping high in the case of any interruption in the V_{IN} generation (if the main converter enters some skip mode or during the system stop). Practically, the input voltage presence is detected by the "SYNC" pin.

Soft–Start

The voltage reference of the error amplifier is internally clamped by the voltage of pin 7. A current source (I_{SS} = 50 μA) flows out of this pin. A capacitor should be applied to pin7 so that during the startup phase, the pin voltage slowly ramps up. As a consequence, the error amplifier output increases in a soft manner. Hence, the high–side MOSFET duty–cycle smoothly increases and as a result, this leads to a soft–start and to a reduction of the stress during this sequence.

A resistor can also be placed between pin 7 and ground to adjust the maximum duty–cycle of the high–side MOSFET. Combine the two functions by implementing these two components in parallel.

If no component is placed in parallel to the capacitor, the soft–start voltage ramps up until the internal clamp is activated. At that moment, the soft–start has no limiting action on the duty–cycle that is only controlled by the error amplifier and if used, by the auxiliary operational amplifier.

OverLapping and Transitions
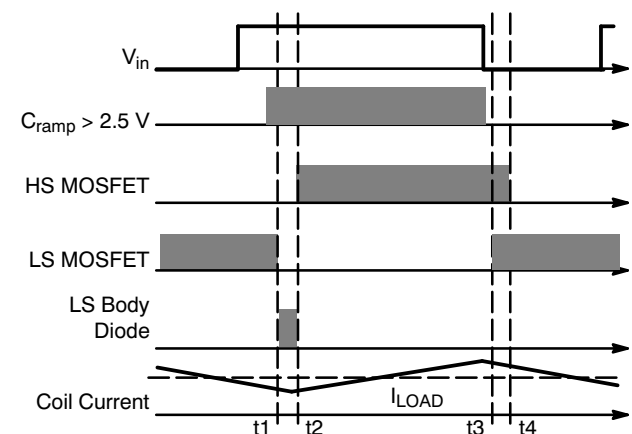
Figure 23. Sequencing and Overlaps Management

As portrayed by Figure 23, three transitions over four are soft:

1. **Low–side Turn On (t3)**: The synchronization block detects when the input voltage (V_{in}) drops to zero and following this event, it resets the circuit to prepare it for the next switching period. Practically, the C_{RAMP} timing capacitor and the PWM latch are re–initialized and the low–side MOSFET is turned on. Just before this low–side transition, the post–regulator input voltage is low and its high–side MOSFET is still on. As a consequence, the low–side MOSFET drain potential is closed to 0 V. Thus the low–side MOSFET turns on in a Zero Voltage Switching mode (ZVS). Hence, the energy Qg necessary to

turn on the low-side MOSFET is significantly minimized (no Miller plateau) and the switching losses are very low.

2. **Low-side Turn Off (t1)**: The high-side MOSFET turns on about 70 ns after the low-side opening. During this 70 ns time when both switches are off, the body diode of the low-side MOSFET derives the coil current (in nominal load condition, when the coil current is positive, i.e., when it flows toward the output). As a result, the low-side MOSFET turns off while its drain-source voltage keeps around zero due to its body diode activation. Again, the energy Qg to be extracted for opening the low-side MOSFET is small and the switching losses are low.

3. **High-side Turn Off (t4)**: The low-side MOSFET turns on 70 ns before the high-side MOSFET turns off. Hence, just before t4, the input voltage being low and the low-side MOSFET being on, the voltage across the high-side MOSFET is nearly zero while the low-side MOSFET generally already derives the major part of the coil current. Finally, this transition is very soft (low current, no voltage)

Only the high-side turn on (t2) that leads to switch the full current and voltage, is "hard". This sequencing that makes soft 3 transitions over 4, helps maximize the efficiency of the post-regulator.

Other Drive Constraints

The post-regulator is the seat of large "dV/dt" that may disturb the system operation if the drivers are not strong enough to contain them. There are two "dV/dt" the circuit must face:

1. When the high-side MOSFET turns on, the potential of the "HB" node sharply increases and hence, it produces a huge current through the C_{rss} capacitor of the low-side MOSFET. This current

may lead to a parasitic turn on of the low-side MOSFET if the driver impedance is too high to absorb this current without a significant increase of the driver voltage. For instance, a 30 V / 10 ns dV/dt produces a 450 mA current through a 150 pF C_{rss} (450 = 150 pF • (30 V / 10 ns)). If the driver voltage must keep below 2.5 V to prevent unwanted turn on, the driver sink resistor should be less than: $R_{sink} = (2.5 \text{ V}/0.45 \text{ A}) = 5.5 \text{ }\Omega$.

2. Similarly, the sink capability of the high-side driver must be high enough to face the high dV/dt that occurs when the post-regulator input voltage abruptly turns high. Again, a 30 V / 10 ns dV/dt would produce a 450 mA current through a 150 pF C_{rss} and the driver sink resistor should be less than: $R_{sink} = 5.5 \text{ }\Omega$.

Finally, the immunity to (dV/dt)s is the main criterion in the dimensioning of the driver sink capability. Both the low and high side drivers that features a 4 Ω maximal sink resistance, allows a robust post-regulator operation.

It must be noted that the drivers remain in a sinking mode whenever the circuit is off following an Undervoltage Lockout condition, the activation of the thermal shutdown or an undervoltage condition.

Synchronization Block

The "SYNC" pin is designed to receive the post-regulator input voltage ("V_{in}" of the application schematic). When this voltage drops below the 2.5 V internal threshold, the circuit generates a "RESET" pulse signal that is long enough (about 250 ns) to:

- Activate the internal switch that is implemented to ground and fully discharge the C_{RAMP} timing capacitor. The circuit is then initialized for a next cycle.

- Reset the PWM latch and hence, initiate a free-wheeling phase (the circuit turns on the low-side MOSFET and 70 ns later, it opens the high-side MOSFET).
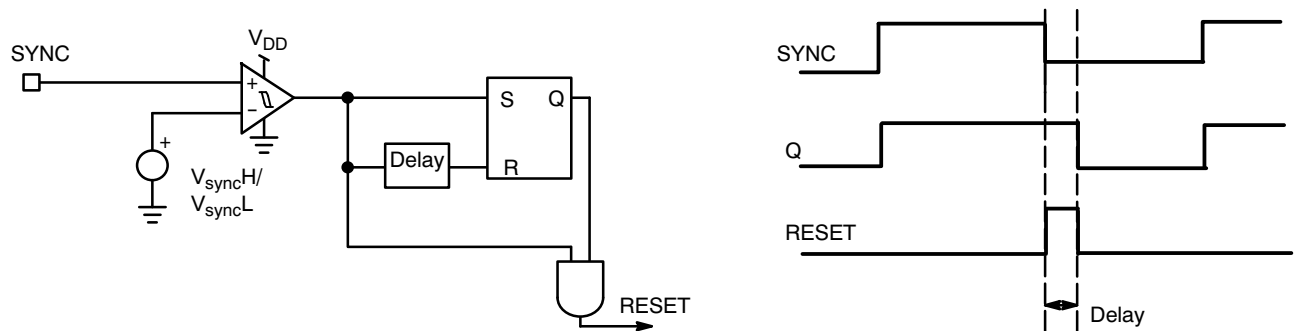
Figure 24. Synchronization Block

The synchronization block generates a short reset pulse. Its duration ("delay") is 250 ns typically.

The voltage that is applied to the "SYNC" pin, may be slightly negative during one part of the period. The NCP4331 incorporates a negative protection system that

clamps the negative spikes that may cause an improper operation of the circuit. The protection is fully effective as long as the pin 16 source current is kept below 2 mA.

Generally speaking the pin voltage is clamped to be between −100 mV and 10 V. It is recommended to apply the synchronization signal ("V_{in}" typically) through a resistor so that the current absorbed and sourced by the pin clamp network stays in the range of 1 mA.

Bootstrap Pin

The circuit features a bootstrap pin ("BST") to optimally drive the high-side N−MOSFET. A 0.1 μF to 1 μF ceramic capacitor should be connected between this pin and the 'HB' node that is connected to the source of the high-side MOSFET. The "BST" voltage feeds the high-side driver ("HS_DRV"). Practically, the V_{DD} voltage is applied to the "BST" pin through a diode (see application schematic of page 1) so that the bootstrap capacitor is charged to V_{DD} when the "HB" pin is low (when the low-side MOSFET conducts). Hence, some voltage source referenced to the "HB" node (and then to the high-side MOSFET source) is made available for an effective control of the high-side MOSFET.

Internal Voltage Regulator

The circuit incorporates a voltage regulator to ease the circuit feeding. Pin 16 makes the input of this regulator available. It can receive a dc voltage (up to 30 V). This voltage is post−regulated down to 9 V to provide the V_{DD} voltage that supplies the circuit.

Undervoltage Lockout (UVLO)

An under−voltage lockout comparator is incorporated to guarantee that the device is properly supplied before enabling the output stages. The NCP4331 starts to operate when the power supply V_{DD} exceeds 6.0 V. A 0.4 V hysteresis avoids erratic turning on and off of the device. Also, a post−regulator having to operate in a noisy environment, a 30 μs blanking time avoids that an UVLO is

detected because of a spike or of some noise. When the NCP4331 detects an under−voltage lockout condition, the "fault" flag is asserted and both the high−side and low−side drivers are forced off.

A minimum V_{CC} voltage must be present (at least 3 V) to ensure the active grounding of the drivers. If V_{CC} is lower, the drivers may be only tied to ground by a 60 kΩ internal resistor

The undervoltage lockout has a 5 V minimum threshold (falling). As a consequence, 5 V minimum are available to drive the power switch. Such a level generally allows an efficient drive of most MOSFETs.

Undervoltage Protection (UVP)

This pin is designed to receive a low inertia voltage representative of the input voltage magnitude, in order detect too low input voltage pulses and to turn off both the low−side and high−side drivers in such a faulty condition. The soft−start pin is grounded when an UVP condition is detected so that the circuit smoothly recovers operation when the fault disappears. In addition to the permanent 60 mV hysteresis of the UVP comparator, this block sources 25 μA out of pin4 when no UVP is detected, to further increase the hysteresis as much as necessary to avoid erratic turns on and off of the device.

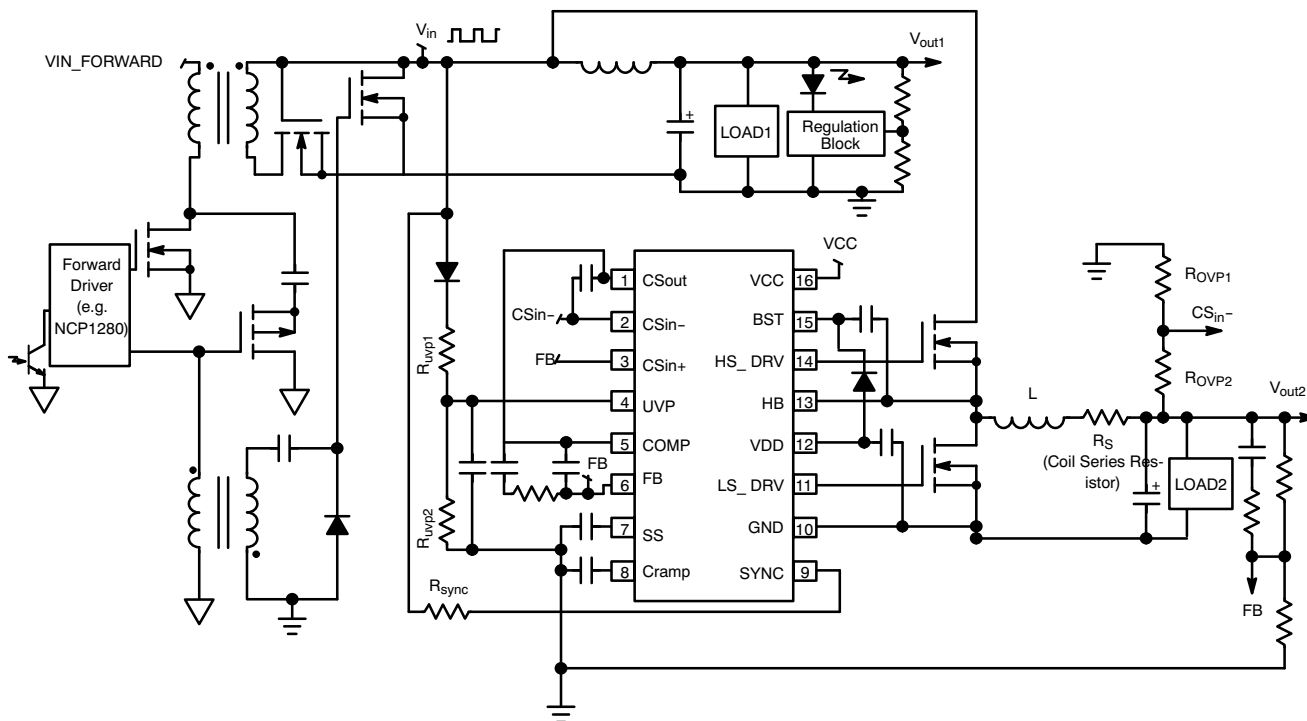A 5 μs blanking time avoids inappropriate UVP detection that may result from the application noise.

Thermal Shutdown (TSD)

The NCP4331 senses its junction temperature. When it exceeds 150°C, the circuit turns low both the high−side and low−side drivers. The power switches are kept off until the temperature has dropped to about 100°C (50°C hysteresis). Like the Undervoltage Lockout block, the TSD incorporates a 30 μs blanking time to avoid any false detection that may result from noise.

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Figure 25. "Basic" Configuration (No Use of the Auxiliary Operational Amplifier)

The input voltage (V_{IN}) is rectified and a portion of the resulting signal is applied to the UVP pin so that the NCP4331 stops operating when V_{IN} is too low. The low and high thresholds of the UVP comparator set the V_{IN} limits (V_{IN} rising and falling) together with the V_{CC} capacitor.

Figure 26. "Basic" Configuration Further Including an Overvoltage Protection (OVP)

Compared to the "basic" configuration, Figure 26 further includes an OVP feature that utilizes the auxiliary operational amplifier (OPAMP2). Two resistors R_{ovp1} and R_{ovp2} scale down the output voltage and the resulting portion of V_{out2} is applied to the inverting input of OPAMP2. The non inverting input receives the feedback signal that nominally equates the internal reference voltage (V_{REF}). Hence, V_{REF} also serves as the OVP reference. R_{ovp1} and R_{ovp2} must be dimensioned so that OPAMP2 "triggers" when V_{out2} exceeds its maximum acceptable level. The output of OPAMP2 ("CSout" that is SINK only) is connected to the COMP pin to reduce the duty–cycle in case of OVP. CSout can be connected to the soft-start pin if a low duty–cycle re-start-up is preferred after an OVP event. It can be noted that both options offer a protection if the feedback is accidentally grounded since in this case, the pin6 voltage and hence, the OVP threshold are close to zero. Ultimately, the post–regulator is protected in this fault condition.

NCP4331
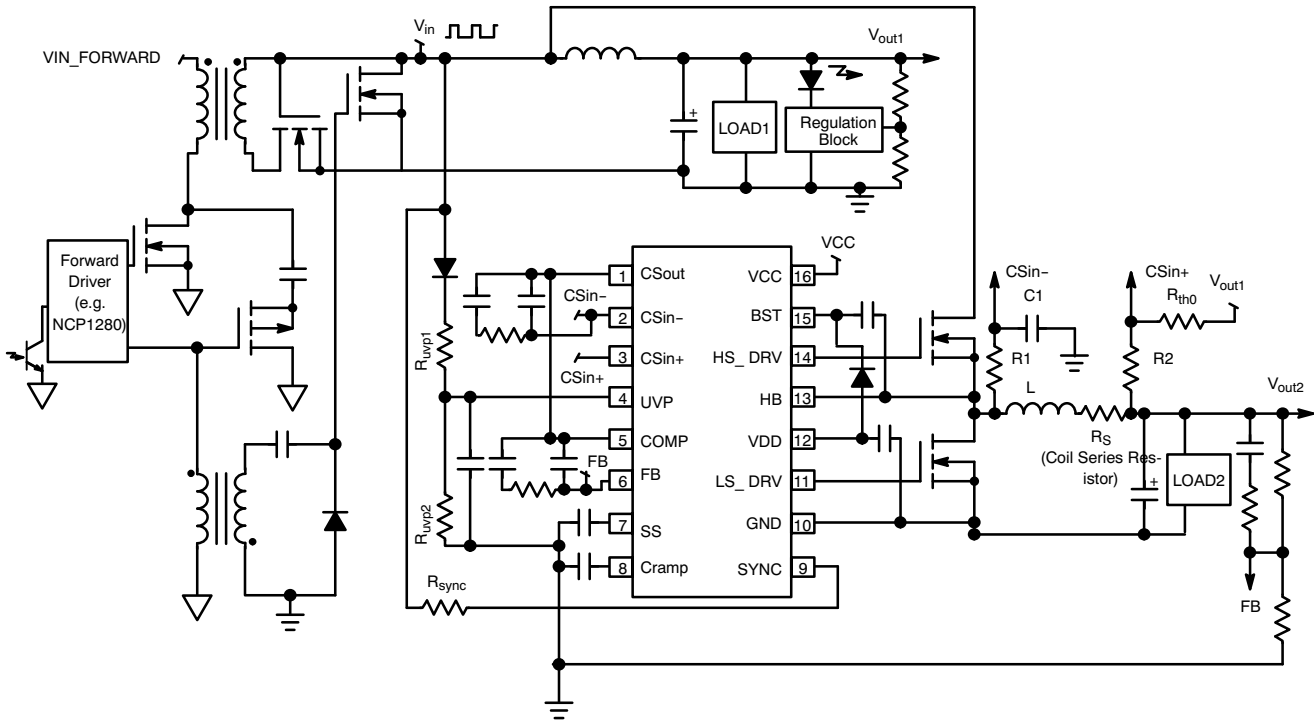
Figure 27. Post–Regulation with CCCV Protection

In Figure 27, the series resistor R_S of the inductor senses the coil current. Practically if the resistors R_1 and R_2 are equal and if R_{th0} is high compared to them, the inductor voltage is integrated by the auxiliary OPAMP. Since the average voltage across the pure inductive part of the coil is zero in steady state, this sensing technique actually returns the averaged voltage across the series resistor R_S ("V_{RS}"). V_{RS} is compared to an offset created using the main output voltage ("V_{out1}") together with of the R2 and Rth0 resistors (more specifically, this offset is $[(R2/(R2 + R_{th0})) \bullet V_{out1}]$). Finally, the coil maximum current is given by: $(I_{coil})max = (R2/(R2 + R_{th0})) \bullet V_{out1}/R_S$. Any accurate voltage source could be used instead of V_{out1}. This technique that limits the coil current as a function of the main output V_{out1}, further performs some soft–start function and helps V_{out2} track V_{out1}.
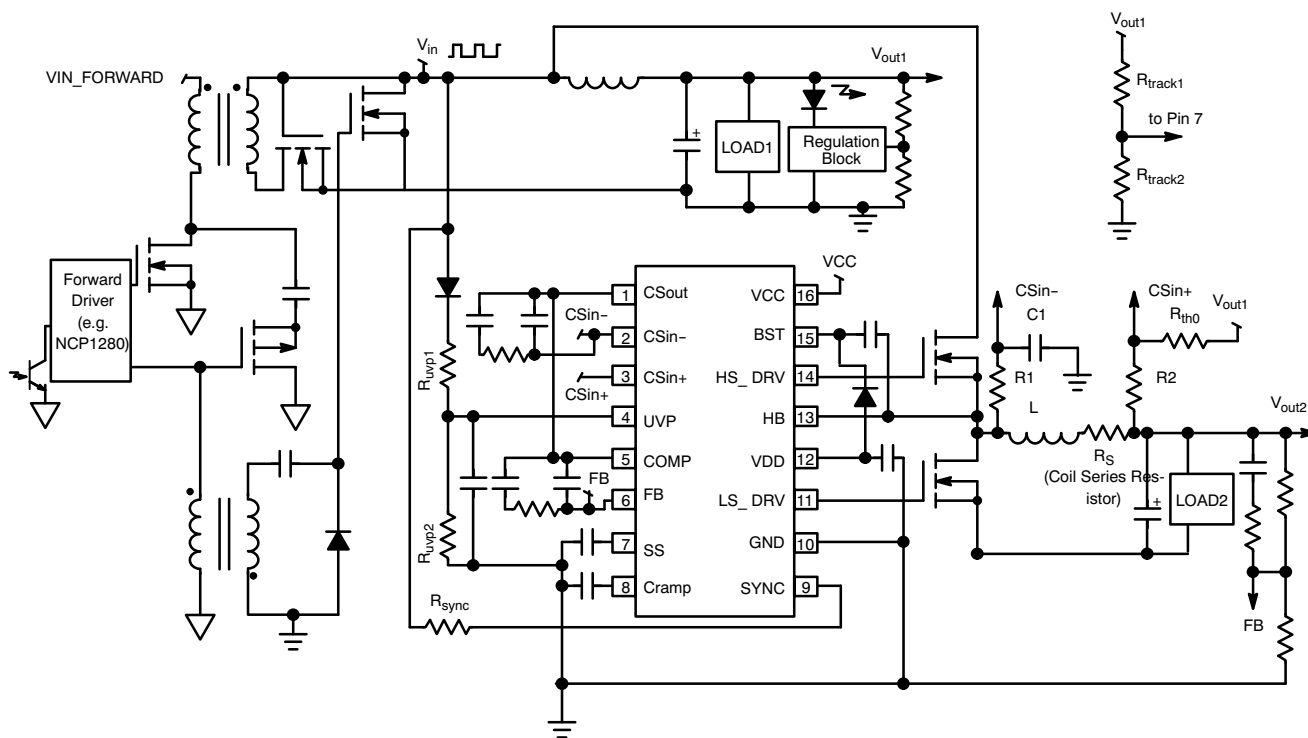
Figure 28. Post–Regulation with CCCV, OVP and Enhanced Tracking of the Main Output Voltage ("V$_{out1}$")

Compared to Figure 27, Figure 28 further consists of the resistors "R$_{track1}$" and "R$_{track2}$" that serve to apply a portion of the main output voltage ("V$_{out1}$") to the NCP4331 soft–start pin. Hence, the post–regulator duty–cycle is limited by the V$_{out1}$ level for an improved tracking.

NCP4331

PACKAGE DIMENSIONS

TSSOP−16
CASE 948F−01
ISSUE B
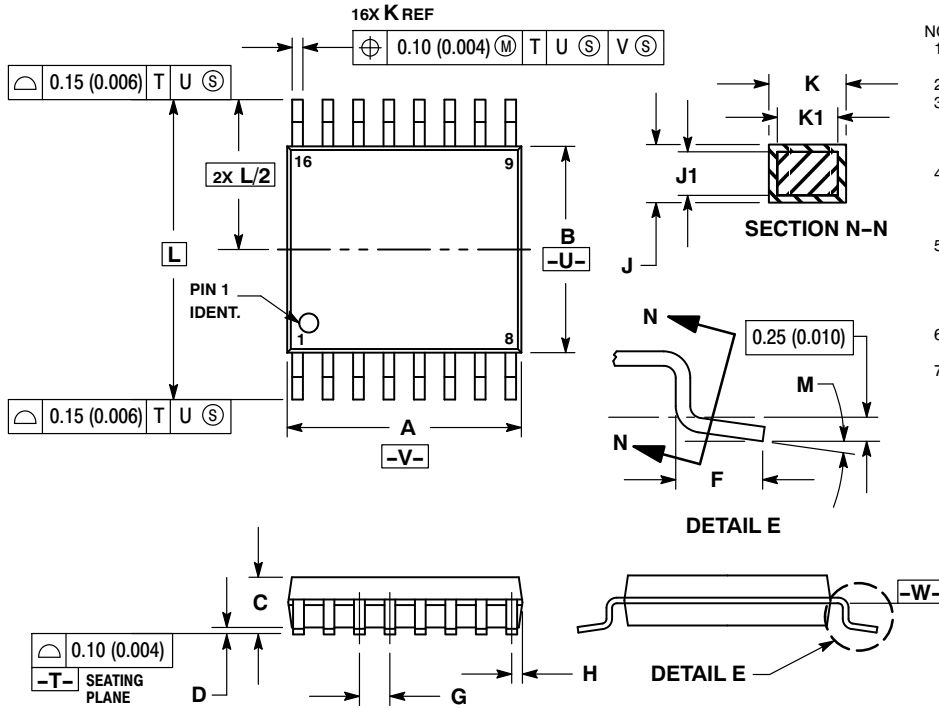
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SECTION N−N
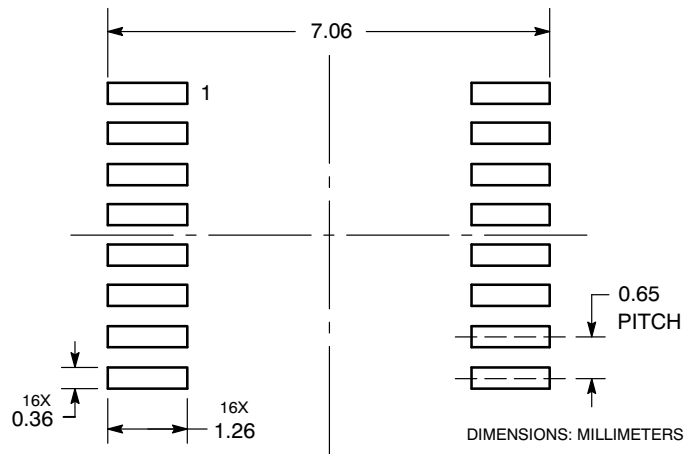
DETAIL E

SOLDERING FOOTPRINT

7.06

0.65 PITCH

16X 0.36

16X 1.26

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NCP4331

PACKAGE DIMENSIONS

SOIC−16
CASE 751B−05
ISSUE K
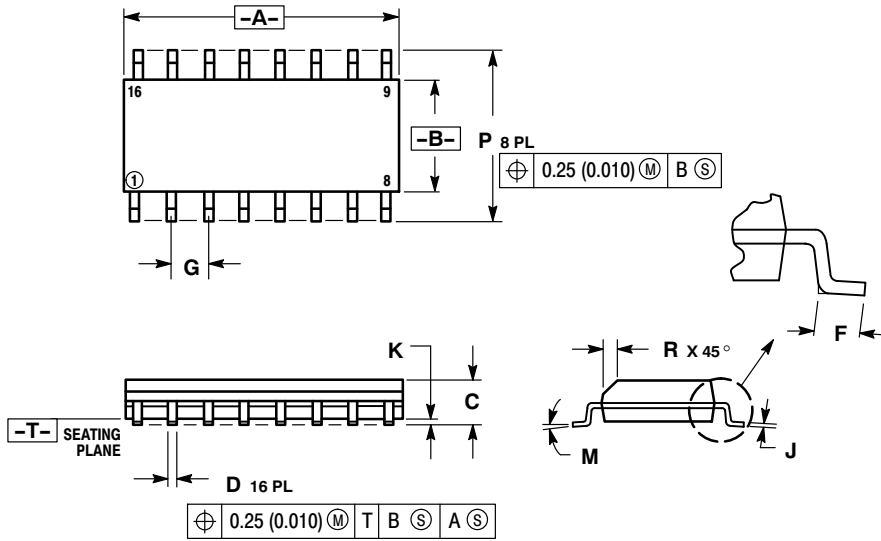
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NCP4331/D